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(74) Agent: DULJVESTIJN, Adrianus, J.; Philips Intellectual  
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Eindhoven (NL).

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CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE,  
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MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT,  
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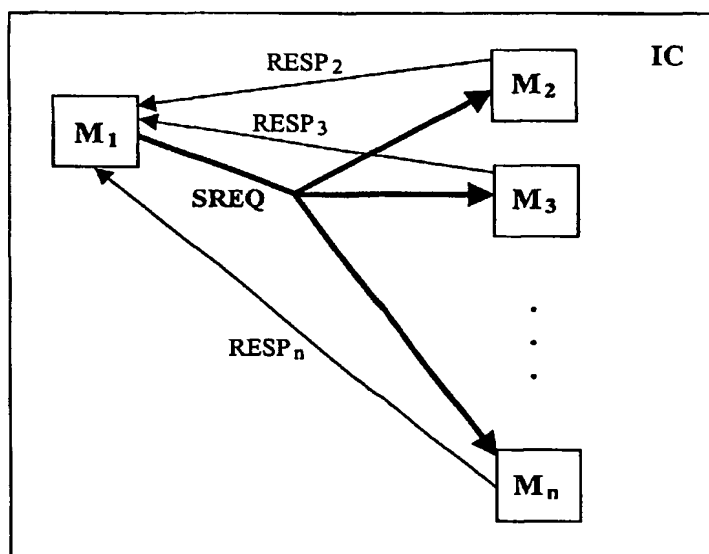
(84) Designated States (*regional*): ARIPO patent (GH, GM,  
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[Continued on next page]

(54) Title: INTEGRATED CIRCUIT AND METHOD FOR SENDING REQUESTS



(57) Abstract: In networks on an integrated circuit a first module typically has access to an address space, wherein addresses identify locations within second modules. It may be necessary to address two or more second modules simultaneously. In that case, the first module replicates a request and sends the resulting plurality of requests to the second modules. This causes a large burden on the first module. The integrated circuit and the method according to the invention overcome this shortcoming, because the network can provide a multicast request to at least two second modules in response to a single request from the first module. For this purpose, the network can comprise a facility to map a multicast address onto two or more further addresses. Alternatively, a connection identifier 10 can be sent along with a request, which identifies a multicast connection.

**Declaration under Rule 4.17:**

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TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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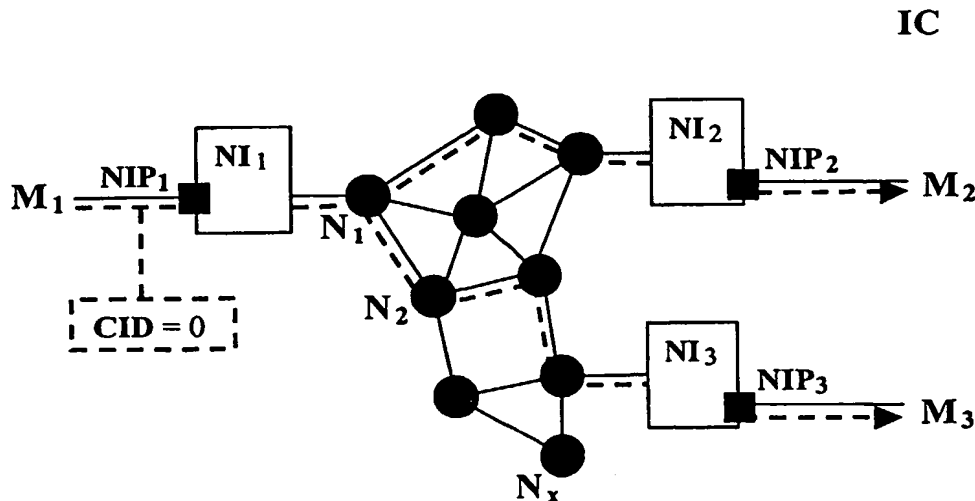
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(72) Inventors; and

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[Continued on next page]

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(57) Abstract: In networks on an integrated circuit a first module (M1) typically has access to an address space (ADDR-SPC), wherein addresses identify locations within second modules. It may be necessary to address two or more second modules (M2) simultaneously. In that case, the first module replicates a request (SREQ) and sends the resulting plurality of requests to the second modules (M2). This causes a large burden on the first module. The integrated circuit and the method according to the invention overcome this shortcoming, because the network can provide a multicast request to at least two second modules (M2) in response to a single request (SREQ) from the first module (M1). For this purpose, the network can comprise a facility to map a multicast address onto two or more further addresses. Alternatively, a connection identifier 10 can be sent along with a request (SREQ), which identifies a multicast connection.

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*DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*

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A. CLASSIFICATION OF SUBJECT MATTER  
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According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 G06F H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	<p>KUMAR S ET AL: "A Network on Chip Architecture and Design Methodology" VLSI ON ANNUAL SYMPOSIUM, IEEE COMPUTER SOCIETY ISVLSI 2002 PITTSBURGH, PA, USA 25-26 APRIL 2002, LOS AALMITOS, CA, USA, IEEE COMPUT. SOC, US, 25 April 2002 (2002-04-25), pages 117-124, XP002263346 ISBN: 0-7695-1486-3 page 119, left-hand column, line 13 -page 120, left-hand column, line 28 page 120, right-hand column, line 1 -page 122, left-hand column, line 6; figures 1-3</p> <p>--- -/--</p>	1-7

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

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International Application No  
PCT/IB 03/04322

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	<p>CHU-SING YANG ET AL: "Building an adaptable, fault tolerant, and highly manageable web server on clusters of non-dedicated workstations" IEEE, 21 August 2000 (2000-08-21), pages 413-420, XP010516422 page 414, left-hand column, line 5 -page 415, right-hand column, line 50; figure 1</p>	1-7
A	<p>GUERRIER P ET AL: "A Generic Architecture for On-Chip Packet-Switched Interconnections" IEEE, 27 March 2000 (2000-03-27), pages 250-256, XP010377472 page 251, right-hand column, line 36 -page 252, right-hand column, line 16 page 254, right-hand column, line 1 -page 255, left-hand column, line 15; figures 2,3</p>	1-7
A	<p>EP 0 935 375 A (NCR INT INC) 11 August 1999 (1999-08-11) paragraph '0130! - paragraph '0133! paragraph '0155! - paragraph '0157!; figure 2</p>	1-3,7

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EP 0935375	A	11-08-1999	US	6256740 B1	03-07-2001
			EP	0935375 A1	11-08-1999
			JP	11316746 A	16-11-1999
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